



## Features

- Solid-state silicon-avalanche technology
- 100 Watts Peak Pulse Power per Line ( $t_p=8/20\mu s$ )
- Low operating and clamping voltages
- Protects five I/O lines
- Working Voltages: 5 V
- Low Leakage Current

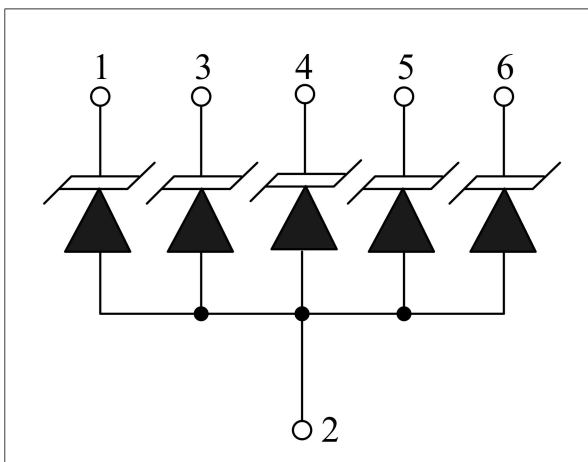
## IEC Compatibility (EN61000-4)

- IEC 61000-4-2 (ESD)  $\pm 15kV$  (air),  $\pm 8kV$  (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)

## Mechanical Characteristics

- SOT-363 package
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code
- Packaging: Tape and Reel
- RoHS Compliant

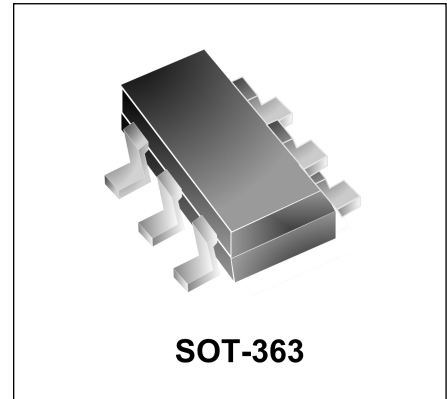
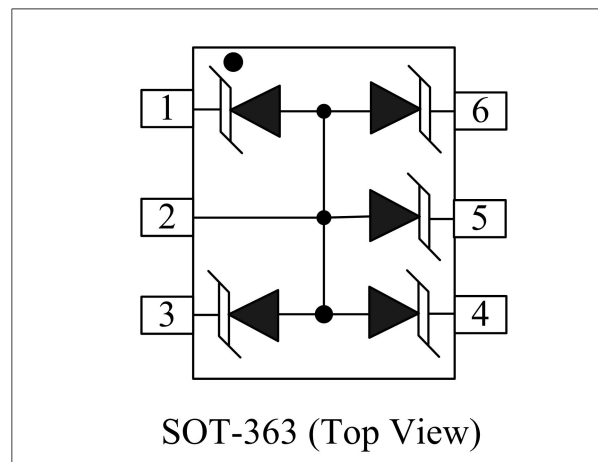
## Circuit Diagram



## Applications

- Cellular Handsets & Accessories
- Personal Digital Assistants (PDAs)
- Notebooks & Handhelds
- Portable Instrumentation
- Digital Cameras
- MP3 Player

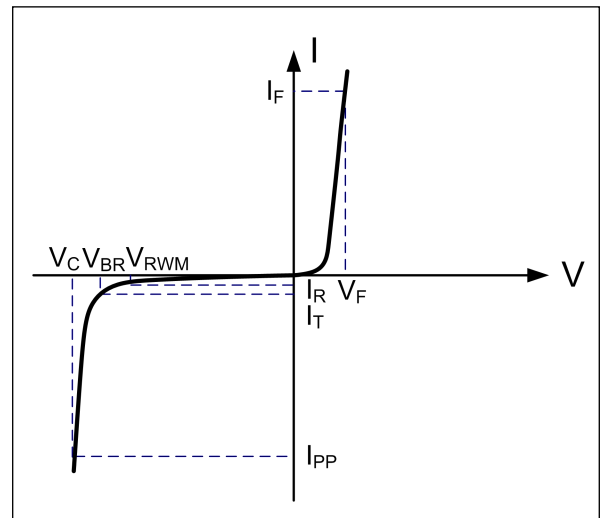
## Schematic & PIN Configuration



Absolute Maximum Rating			
Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p=8/20\mu s$ )	$P_{PP}$	100	Watts
Peak Forward Voltage ( $I_F = 1A, t_p=8/20\mu s$ )	$V_{FP}$	1.5	V
Operating Temperature	$T_J$	-55 to + 125	$^{\circ}C$
Storage Temperature	$T_{STG}$	-55 to +150	$^{\circ}C$

### Electrical Parameters (T=25 $^{\circ}C$ )

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$



### Electrical Characteristics

DW05MFC-S						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$				5.0	V
Reverse Breakdown Voltage	$V_{BR}$	$I_T=1mA$	6.0			V
Reverse Leakage Current	$I_R$	$V_{RWM}=5V, T=25^{\circ}C$			1	$\mu A$
Peak Pulse Current	$I_{PP}$	$t_p=8/20\mu s$			6.5	A
Clamping Voltage	$V_C$	$I_{PP}=1A, t_p=8/20\mu s$			9.5	V
Clamping Voltage	$V_C$	$I_{PP}=6.5A, t_p=8/20\mu s$		13.5	15	V
Junction Capacitance	$C_j$	Between I/O pins and Ground $V_R = 0V, f = 1MHz$		22		pF



### Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

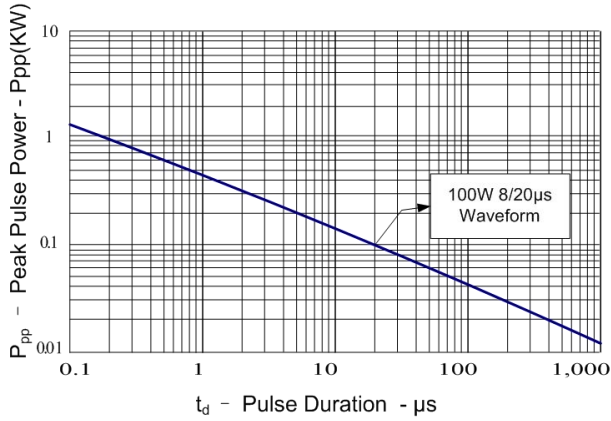


Figure 2: Power Derating Curve

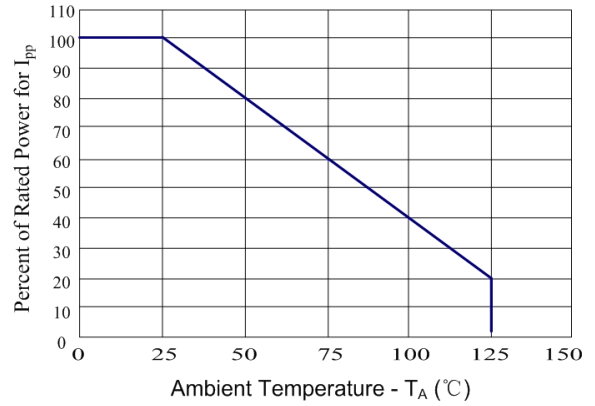


Figure 3: Clamping Voltage vs. Peak Pulse Current

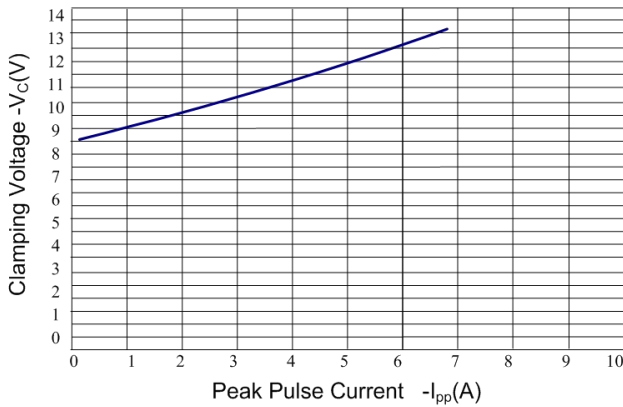


Figure 4: Normalized Junction Capacitance vs. Reverse Voltage

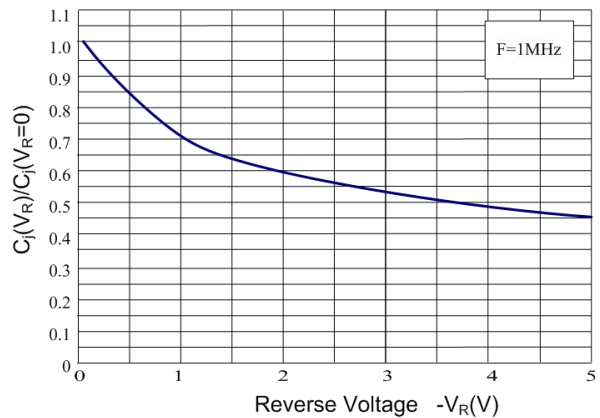


Figure 5: Pulse Waveform

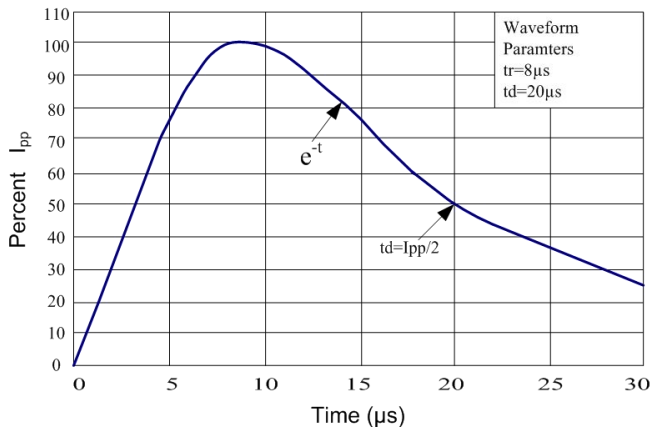
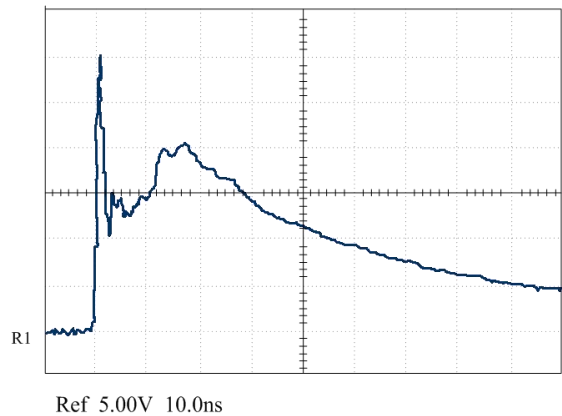


Figure 6: ESD Pulse Waveform (Per IEC 61000-4-2)



## Application Information

The DW05MFC-S Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product provides unidirectional protection; the device is connected as follows:

### BIDIRECTIONAL COMMON-MODE CONFIGURATION

The DW05MFC-S provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 7.

Circuit connectivity is as follows:

- I/O 1 is connected to Pin 3.
- I/O 2 is connected to Pin 1.
- I/O 3 is connected to Pin 6.
- I/O 4 is connected to Pin 4.
- Pin 5 is connected to ground.

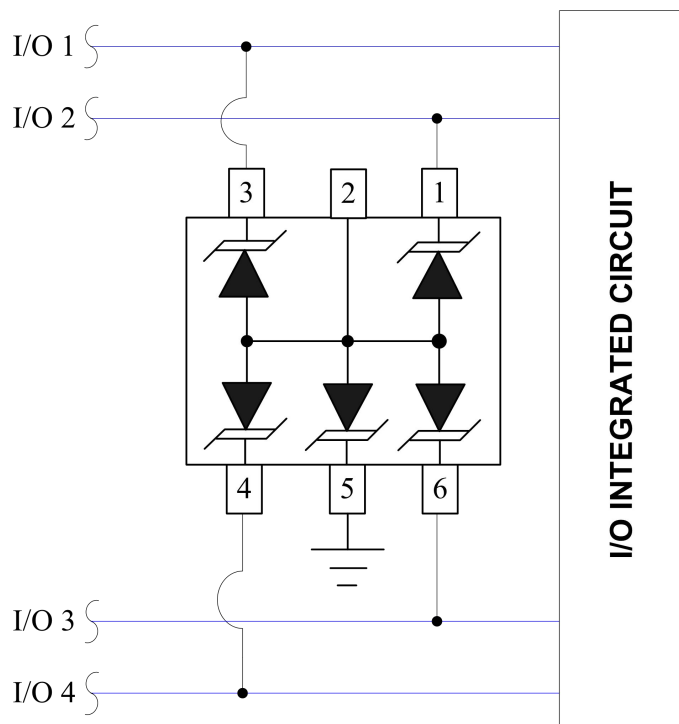


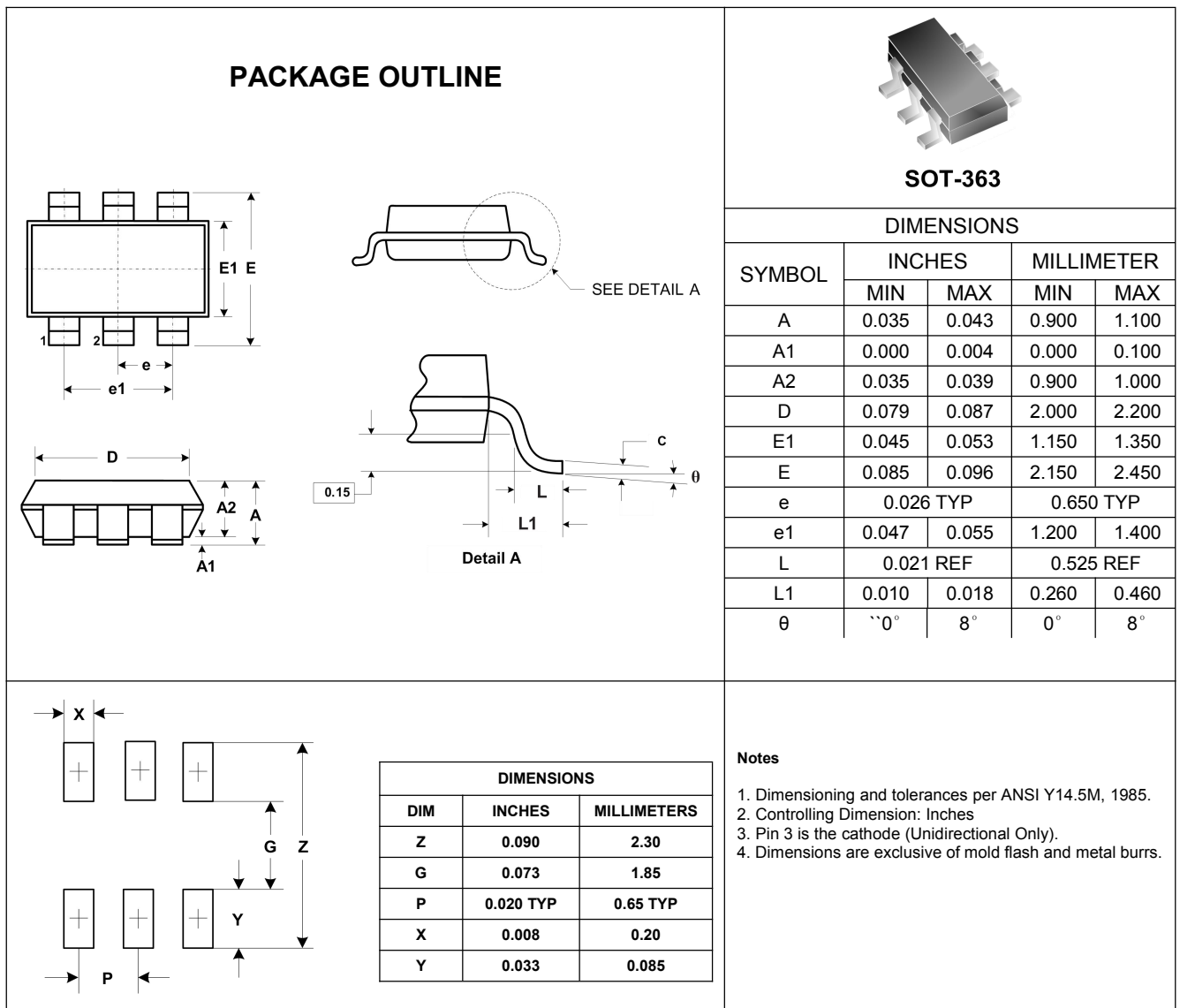
Figure 7 Bidirectional Configuration Common-Mode I/O Port Protections

### CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

## Outline Drawing – SOT-363



## Marking Codes

Part Number	DW05MFC-S
Marking Code	5FC

## Package Information

Qty: 3k/Reel